(54) Title: CONTROL OF BIAS VOLTAGE

(57) Abstract: The invention concerns a method for maintaining an optimal operating point of an LDMOS device (32) stable, said LDMOS device (32) producing an output signal including an error signal component (err). The method comprises separating said error signal component (err) from the output signal of said LDMOS device (32) and using said error signal component (err) for controlling the gate-to-source bias voltage, or Vgs, of said LDMOS device (32) to maintain the optimal operating point of said LDMOS device (32) stable.

Control of Bias Voltage

Field of the Invention

The invention relates to a method and an arrangement for maintaining an optimal operating point of LDMOS semiconductor devices stable.
5   The invention is especially useful in a feedforward amplifier arrangement.

Background of the Invention

Particularly in broadband amplifiers and in power amplifiers, amplifier non-linearities cause distortion to an output signal. Figure 1 illustrates the formation of intermodulation products (IM-products) causing distortion to an
10   output signal. An undistorted input signal 12 consisting of two frequency components $\omega 1$ and $\omega 2$ is fed into an amplifier 14. At the output of the amplifier 14 appears a distorted signal 16, which includes desired signal components at frequencies $\omega 1$ and $\omega 2$ and also two strong undesired signal components close to the desired signal components at the frequencies $2^*\omega 1-\omega 2$ and $2^*\omega 2-$
15    $\omega 1$. These undesired signals may appear in the desired signal band, and thereby corrupt the output signal.

LDMOS (Laterally Diffused Metal Oxide Semiconductor) devices are relatively new semiconductor devices, which have improved characteristics compared to conventional semiconductor devices. For example, they have im-
20   proved IM performance, i.e. they produce less IM-products at the same input power than the conventional semiconductor devices. Typical input power/IM-products curves of a conventional semiconductor device and of an LDMOS device are illustrated in Figure 2 by a dashed line and a solid line, respectively. In a conventional semiconductor device, the amount of IM-products increases
25   as the input power increases. The advantage of an LDMOS device is that it has an optimal operating point called "sweet point" producing an optimal input power/IM-products ratio.

The characteristics of LDMOS devices make them especially well suited for power amplification. However, they are not widely used at the mo-
30   ment. A reason for this is a considerable drift in gate-source bias voltage, or Vgs. The Vgs is a DC voltage which is used to provide a certain drain-source quiescent current, or Idq. The location of the "sweet point" on the input power axis in Figure 2 is dependent on this quiescent current. Therefore, the Vgs can be used to set the "sweet point", i.e. optimal operating point, to the preferred
35   input power level. However, if the Vgs is kept constant, the Idq decreases in

the course of time because of aging of the LDMOS transistors. In other words, the Vgs corresponding to a certain Idq changes in the course of time. This kind of drift in bias voltage due to transistor aging also appears in "normal" semiconductor devices, but it is a considerable problem with LDMOS transistors, in

5   particular. Therefore, a method of keeping the Idq constant is needed for LDMOS devices in order to maintain their "sweet point" at the desired signal level. This object can be achieved by reducing the Vgs drift or by adjusting the Vgs for keeping the Idq constant.

One possible method of reducing the Vgs drift is to "burn in"

10 LDMOS devices before they are used, because the drift phenomenon is most considerable at the beginning of the use of an LDMOS device. The disadvantage of this procedure is that it reduces the lifetime of the device. Additionally, "burn in" is difficult and expensive to implement.

Since the Vgs drift has been reduced from more than 25% to 5% for

15 900 MHz parts and to 12-15% for 2GHz parts by device manufacturers, the problem of the drift has diminished. However, the problem has not disappeared, because a 10% drift may produce 5-10 dB IM-products, which is still relatively much in a linear amplifier.

One proposed method of adjusting the Vgs to keep the Idq con-

20 stant is to measure the Idq and make Vgs adjustments on the basis of the measured Idq. The problem in this kind of an arrangement is that the amplifier has to be shut down during the measurement. Additionally, the transistor characteristics that vary from one transistor to another have an effect on the measurement results.

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Disclosure of the Invention

An object of the present invention is to overcome or alleviate the above described problems by providing a method and an arrangement for keeping the Idq constant in an LDMOS device.

30 The object is achieved by a method and an arrangement which are characterized by what is disclosed in the attached independent claims. Preferred embodiments of the invention are disclosed in the attached dependent claims.In the present invention the bias voltage Vgs of an LDMOS device is adjusted to keep the Idq of the device constant and consequently to maintain an optimal operating point, i.e. the "sweet point", of the device stable. The in-

35 vention employs a method known from a feedforward amplifi r arrangement. A

feedforward amplifier arrangement is one possible solution to achieve high power amplification, high efficiency and low distortion. In a feedforward amplifier arrangement, distortion in the output signal of the arrangement is reduced by separating an error signal component from the output signal of the amplifier

5   and then subtracting this error signal component from the output signal of the amplifier containing the error signal component. Thus, the error signal components cancel each other out and the resulting output signal contains considerably less distortion than the original output signal of the amplifier.

According to the invention, this kind of separate error signal component is used for controlling the Vgs of an LDMOS device to maintain the optimal operating point of the LDMOS device stable. The absolute value of the error signal component at the output of the LDMOS device is defined and the Vgs is adjusted in response to this error signal component so that the error signal component at the output of the LDMOS device reaches its minimum.

15   This invention provides a simple way to control the operating point of LDMOS devices. The invention suits especially well for a feedforward amplifier arrangement, since it employs an error signal that is already generated in a feedforward arrangement and therefore, only few extra components are needed. An advantage of a preferred embodiment of the invention is also that

20   the amplifier does not need to be completely shut down during the Vgs adjustment.

Brief Description of the Drawings

In the following, the invention will be described in greater detail by

25   means of preferred embodiments with reference to the accompanying drawings, in which

Figure 1 illustrates formation of IM-products,

Figure 2 illustrates typical input power/IM-products curves of a conventional semiconductor device and of an LDMOS device,

30   Figure 3A is a block diagram illustrating an arrangement according to the invention,

Figure 3B is a block diagram illustrating an embodiment according to the invention,

Figure 4 is a block diagram illustrating another embodiment according to the invention,

35   cording to the invention,

Figure 5 is a flow chart illustrating the operation of the Vgs control block according to the invention.

Detailed Description of the Invention

5   The present invention can be applied to bias voltage control of an LDMOS device. In the following, the preferred embodiments of the invention will be described by means of a feedforward arrangement, but the invention is not limited to a feedforward arrangement. The same reference numerals are used for equivalent components in the figures.

10   Figure 3A illustrates a block diagram of an arrangement according to the invention including an LDMOS device 32, error signal separating means 30 and Vgs control means 39. The LDMOS device 32 receives an input signal In and produces, on the basis of this input signal In, an output signal including distortion. This output signal of the LDMOS device is connected to the error

15   signal separating means 30 together with the input signal In. The error signal separating means 30 produce an error signal component err which is connected to the Vgs control means 39. On the basis of the error signal component err, the Vgs control means adjust the Vgs of the LDMOS device 32 to keep the operating point of the LDMOS device 32 stable.

20   Figure 3B illustrates an embodiment of the invention including a basic feedforward arrangement 31 and Vgs control means 39. The feedforward arrangement includes an LDMOS amplifier 32, attenuation means 35, time (delay) adjusting means 33 and 36, adders 34 and 37 and an error signal amplifier 38. An input signal In is connected to an input of the LDMOS amplifier

25   32. For obtaining an error signal component err, the input signal is adjusted in time (delayed) with time adjusting means 36 for producing signal A and the output signal of the LDMOS amplifier 32 is attenuated with attenuation means 35 for obtaining signal B. In this way, signals A and B, which are fed into the adder 37, have equal amplitudes and a 180° phase difference relative to each

30   other, and the error signal component err is obtained as an output of the adder 37. For obtaining an output signal Out, in which the error signal component is canceled, the error signal component err is amplified by the error signal amplifier 38 for obtaining signal C and the output signal of the LDMOS amplifier 32 is adjusted in time (delayed) with time adjusting means 33 for obtaining signal

35   D. In this way, signals C and D, which are fed into the adder 34, have equal amplitudes and a 180° phase difference relative to each other, and the output

signal Out, in which the error signal component is canceled, is obtained as an output of the adder 34.

        According to the embodiment shown in Figure 3, the error signal component err is also connected to the Vgs control means 39. The Vgs control

5   means produce the Vgs for the LDMOS amplifier 32 on the basis of the error signal component err, as will be described later in connection with Figure 5.

        Figure 4 illustrates another embodiment of the invention including a feedforward arrangement 40 and Vgs control means 39. The feedforward arrangement 40 includes an LDMOS amplifier 32, adders 34 and 37, time

10   (delay) adjusting means 33 and 36 and an error signal amplifier 38, all of which operate essentially in the same way as in the arrangement of Figure 3B. Gain/phase adjustment means 41 are added for adjusting the phase φ and gain A of the input signal In before amplification. Additionally, the arrangement 40 includes down converter means 44 for converting the error signal and the

15   input signal to a lower frequency, and A/D converters 45 and 46 for converting respective downconverted signals to a digital form for digital signal processing. In response to the output signals of the A/D converters 45 and 46, signal processing means 47 produce a control signal which is connected to adjustment means 41 via sample & hold means 48 and a D/A converter 49.

20   The error signal component err obtained as an output of the A/D converter 45 is also connected to the Vgs control means 39. The Vgs control means produce the Vgs for the LDMOS amplifier 32 on the basis of the error signal component err. The error signal component err is handled in digital domain by the Vgs control means, and the Vgs is produced in a digital form and

25   then converted to an analog form by the Vgs control means.

        The operation of the adjustment means in Figures 3B and 4 must not be changed during the Vgs adjustment, but otherwise the LDMOS amplifier 32 can be operated normally. In other words, the LDMOS amplifier does not have to be completely shut down during the Vgs adjustment.

30   Figure 5 is a flow chart illustrating the operation of a possible implementation of the Vgs control means 39 in Figures 3 and 4. This implementation tries several Vgs values, each attempt having an attempt number N. In step 51, the power level of the Nth error signal err(N) is measured. Then Vgs is increased in step 52 and the power level of the (N+1)th error signal err(N+1)

35   is measured in step 53. In step 54, the power levels of Nth and (N+1)th error signal are compared and, if err(N) > err(N+1), N is incremented in step 55 and

steps 52 to 54 are repeated. Otherwise, the Vgs is first decreased to the value corresponding the Nth error signal in step 56 and then decreased again in step 57. Next, the power level of the (N+1)th error signal err(N+1) is measured in step 58, and the power levels of Nth and (N+1)th error signal are compared in step 59. If err(N) > err(N+1), N is incremented in step 60, and steps 57 to 59 are repeated. Otherwise, the Vgs is increased to the value corresponding the Nth error signal in step 61, and the operation is terminated in step 62.

The description only illustrates preferred embodiments of the invention. The invention is not, however, limited to these examples, but it may vary within the scope of the appended claims.

Claims

1. A method for maintaining an optimal operating point of an LDMOS device (32) stable, said LDMOS device (32) producing an output signal including an error signal component (err), said method comprising

5   separating said error signal component (err) from the output signal of said LDMOS device (32),

c h a r a c t e r i z e d by

using said error signal component (err) for controlling the gate-to-source bias voltage, or Vgs, of said LDMOS device (32) to maintain the opti-

10   mal operating point of said LDMOS device (32) stable.

2. A method according to claim 1, c h a r a c t e r i z e d in that controlling said Vgs comprises the step of

setting different values to said Vgs until the error signal component (err) reaches its minimum.

15   3. A method according to claim 1 or 2, c h a r a c t e r i z e d by using said method in a feedforward amplifier arrangement.

4. A method according to any of claims 1 to 3, c h a r a c t e r i z e d by

controlling the bias voltage without shutting the LDMOS device (32)

20   completely down.

5. An arrangement for maintaining an optimal operating point of an LDMOS device (32) stable, said arrangement comprising

said LDMOS device (32) for receiving an input signal and for producing an output signal based on the input signal, the output signal including

25   an error signal component (err), and

error signal separating means (30) for separating an error signal component (err) from said output signal,

c h a r a c t e r i z e d in that said arrangement further comprises

gate-to-source bias voltage, or Vgs, control means (39) for receiving

30   said error signal component (err) as an input and for adjusting the Vgs responsive to said error signal component (err) and for providing the Vgs to said LDMOS device (32) to maintain the optimal operating point of said LDMOS device (32) stable.

6. An arrangement according to claim 5, c h a r a c t e r i z e d in

35   that

the Vgs control means (39) are adapted to operate without shutting the LDMOS device completely down.

7. An arrangement according to claim 5 or 6, c h a r a c t e r i z e d in that the arrangement is located in a feedforward amplifier arrangement.

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8. An arrangement according to any one of the claims 5 to 7, c h a r a c t e r i z e d in that

the arrangement is part of a multicarrier amplifier.

Fig 1
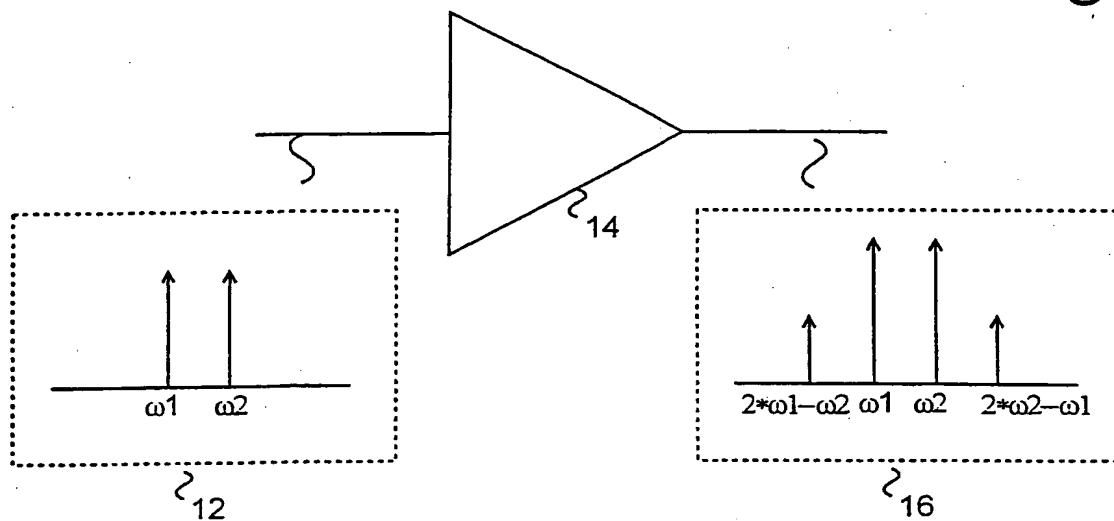
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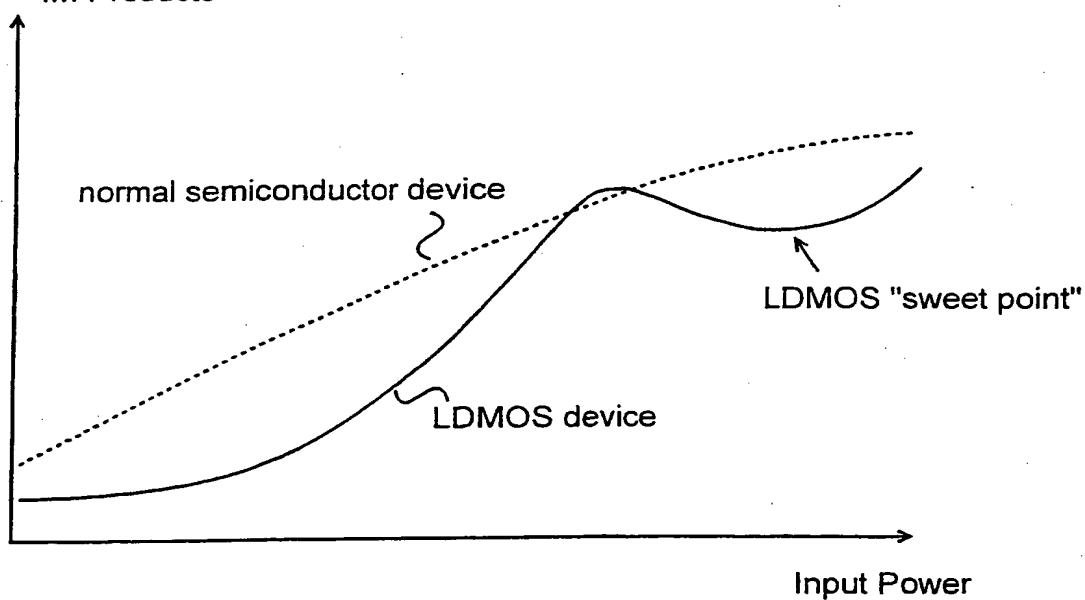
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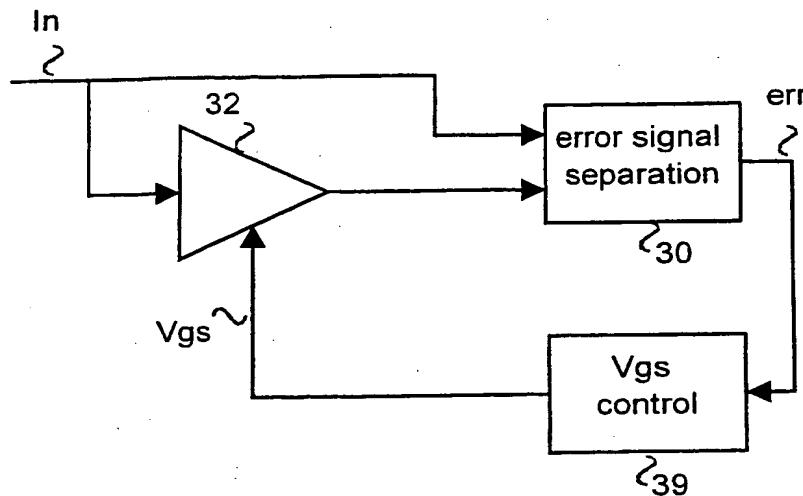
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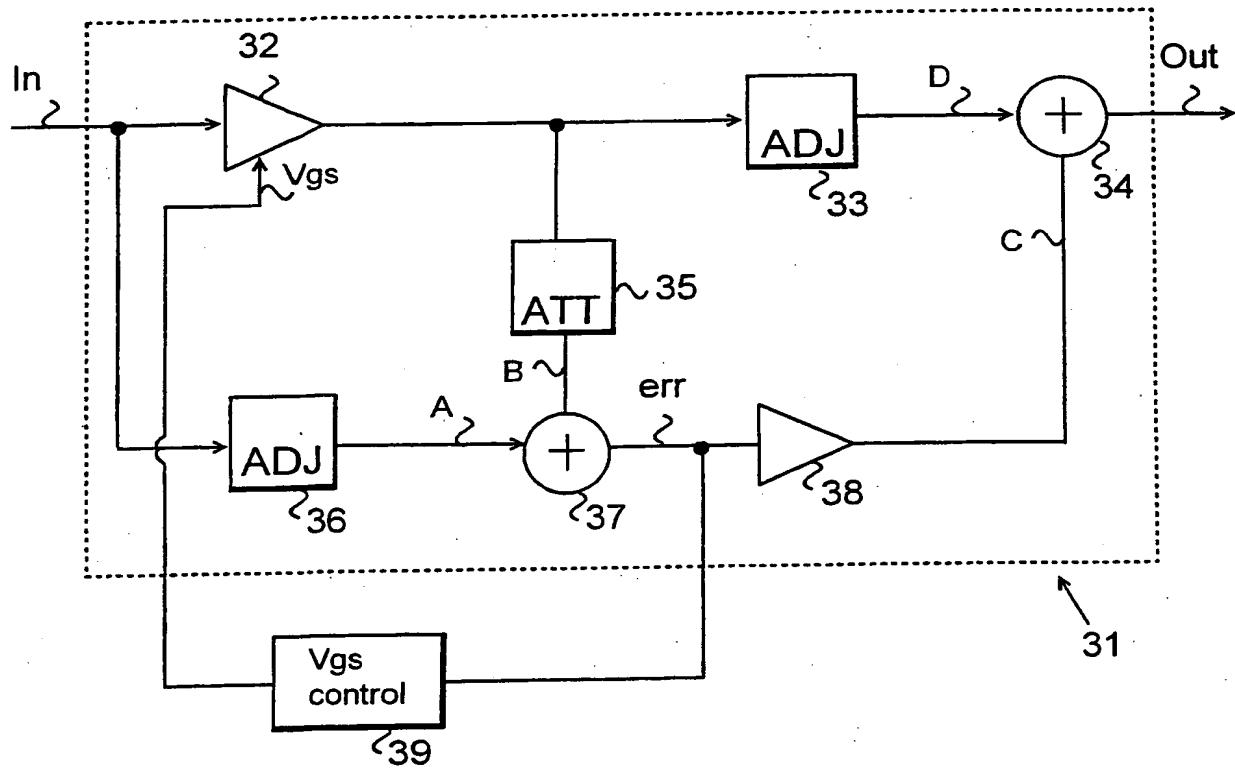
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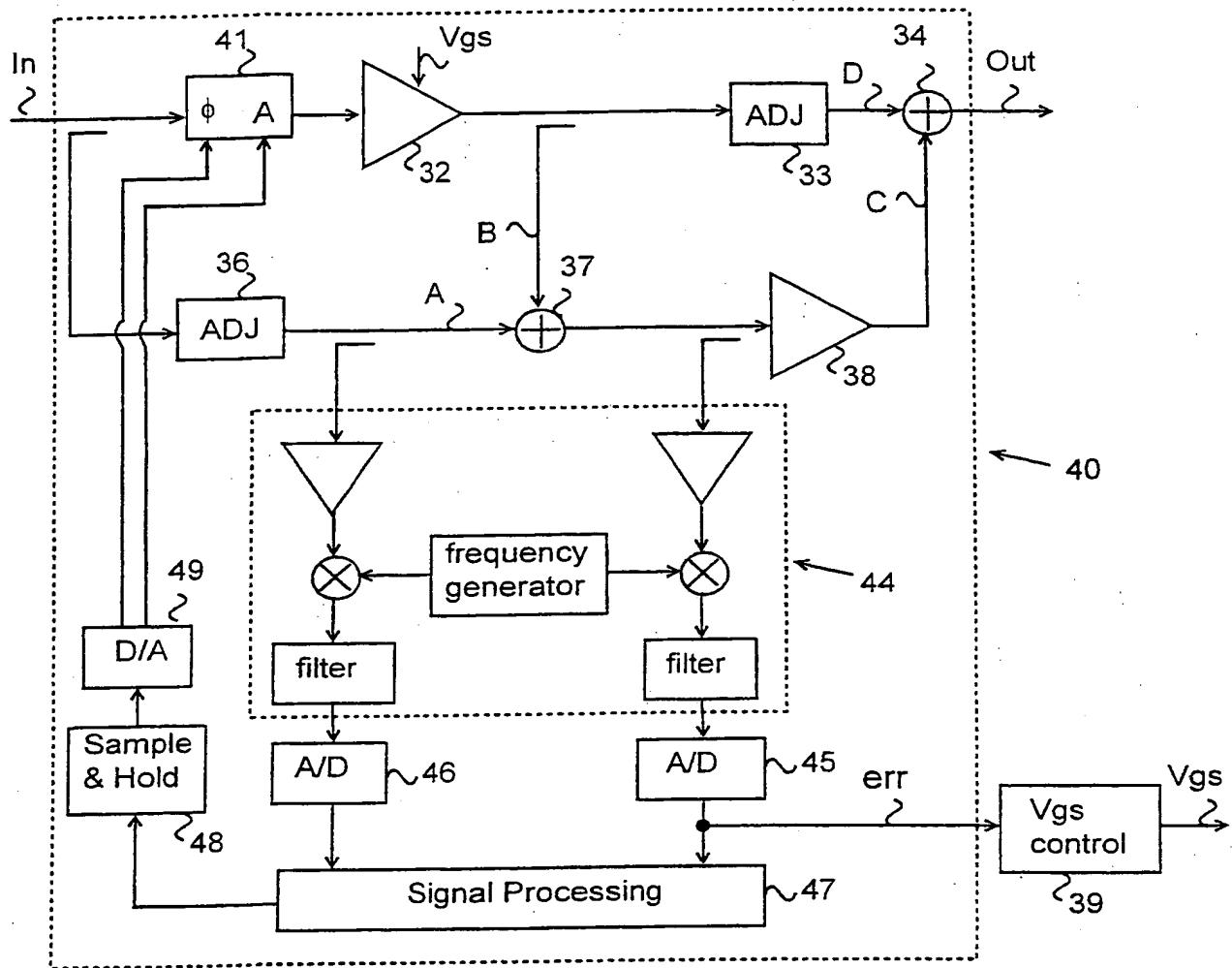
Fig 5
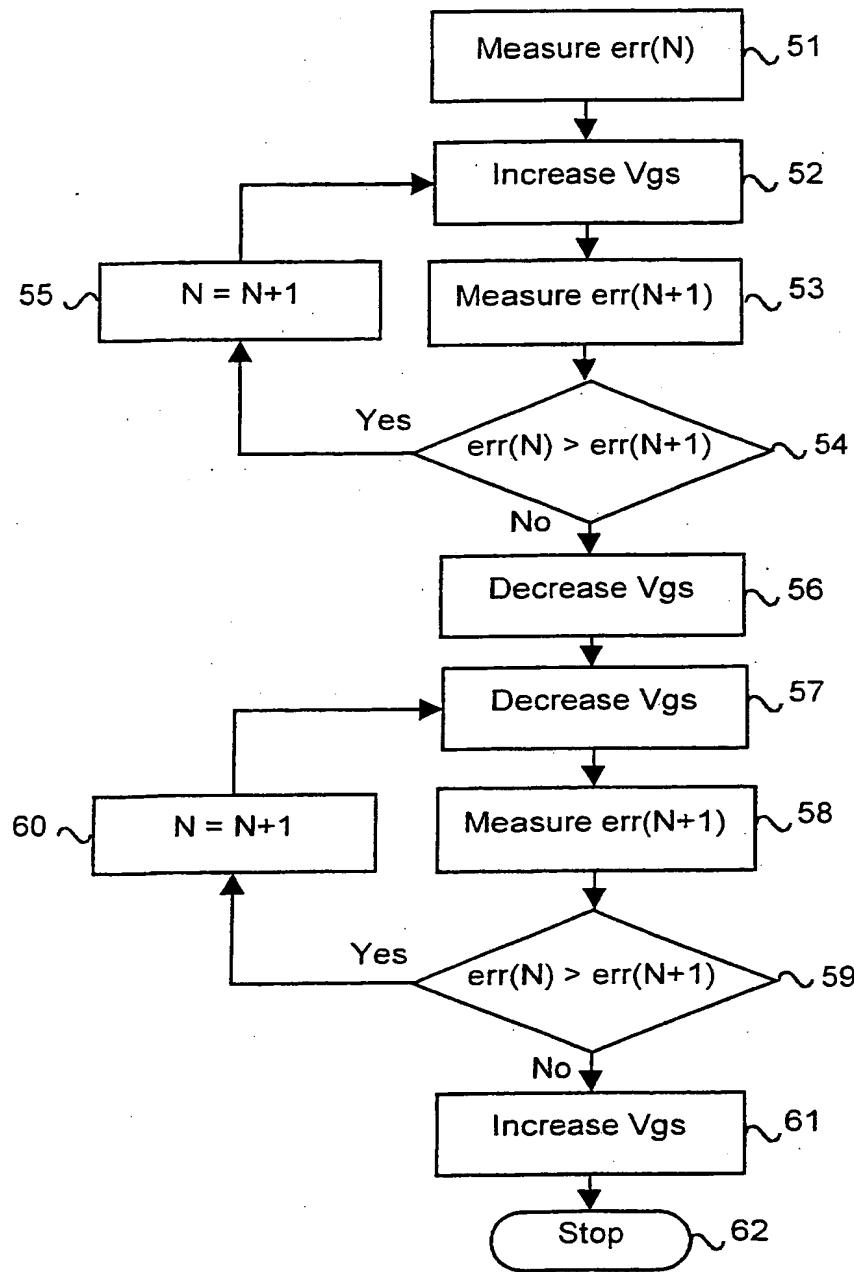
INTERNATIONAL SEARCH REPORT

A. CLASSIFICATION OF SUBJECT MATTER

IPC7: H03F 1/26, H03G 3/30

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC7: H03F, H03G

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

SE,DK,FI,NO classes as above

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
P,Y	US 6069530 A (JOSEPH LYNN CLARK), 30 May 2000 (30.05.00), column 1, line 12 - column 3, line 29, figure 1	1-8
P,Y	US 6111464 A (STEVEN J. LAUREANTI), 29 August 2000 (29.08.00), column 1, line 12 - column 2, line 67	1-8
P,A	US 6107880 A (MICHAEL JOSEPH SHAW), 22 August 2000 (22.08.00), column 1, line 12 - column 2, line 43	1-8
A	US 5973564 A (VADIM V. IVANOV), 26 October 1999 (26.10.99), column 2, line 3 - column 3, line 11	1-8

| X | Further documents are listed in the continuation of Box C. | | X | See patent family annex. |

Date of the actual completion of the international search	Date of mailing of the international search report
22 March 2001	3 0 -03- 2001

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C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	WO 9423491 A1 (QUALCOMM INCORPORATED), 13 October 1994 (13.10.94), page 5, line 1 - page 6, line 11	1-8

INTERNATIONAL SEARCH REPORT
Information on patent family members

25/02/01

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